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Claims

[c1] 1. A method of calculating critical area in an integrated circuit design, said method comprising:

inputting an integrated circuit design;

associating variables with the positions of edges in said integrated circuit design; and

associating cost functions of said variables with spacing between said edges in said integrated circuit design;

wherein said cost functions calculate critical area contributions as the positions and length of said edges in said integrated circuit design change, and

wherein said critical area contributions comprise a measure of electrical fault characteristics of said spacing between said edges in said integrated circuit design.

[c2] 2. The method in claim 1, wherein said process of associating said cost functions comprises mapping points in said spacing between said edges in said integrated circuit design up to when the size of defects located at said points triggers an electrical fault between said edges in said integrated circuit design, wherein said mapping

forms Voronoi cells.

[c3] 3. The method in claim 2, wherein said process of associating said cost functions further comprises using a normal vector representing said Voronoi cells defined in terms of said variables.

[c4] 4. The method in claim 1, wherein said process of associating said cost functions further comprises identifying Voronoi bisectors where Voronoi cells meet.

[c5] 5. The method in claim 4, wherein said Voronoi bisectors are defined by vertices at the ends of said Voronoi bisectors; and wherein said vertices are defined in terms of said variables.

[c6] 6. A method of optimizing critical area in an integrated circuit design, said method comprising:

a) inputting an initial integrated circuit design;

b) associating variables with the positions of edges in said integrated circuit design;

c) associating cost functions of said variables with spacing between said edges in said integrated circuit design;

d) optimizing said positions and length of said edges in said integrated circuit design to reduce critical area contribution cost in a first direction across said

integrated circuit design to produce a revised integrated circuit design; and

e) repeating steps b-d with said revised integrated circuit design in a second direction.

[c7] 7. The method in claim 6, wherein said process of associating said cost functions comprises mapping points in said spacing between said edges in said integrated circuit design up to when the size of defects located at said points triggers an electrical fault between said edges in said integrated circuit design, wherein said mapping forms Voronoi cells.

[c8] 8. The method in claim 7, wherein said process of associating said cost functions further comprises using a normal vector representing said Voronoi cells defined in terms of said variables.

[c9] 9. The method in claim 6, wherein said process of associating said cost functions further comprises identifying Voronoi bisectors where Voronoi cells meet.

[c10] 10. The method in claim 9, wherein said Voronoi bisectors are defined by vertices at the ends of said Voronoi bisectors; and wherein said vertices are defined in terms of said variables.

[c11] 11. The method in claim 10, wherein said cost function

calculates critical area contributions of said Voronoi bi-sectors as said variables change as the layout of said in-tegrated circuit design changes.

[c12] 12. A method of optimizing critical area in an integrated circuit design, said method comprising:

a) inputting an initial integrated circuit design;

b) associating variables with the positions of edges in said integrated circuit design;

c) associating cost functions of said variables with spacing between said edges in said integrated circuit design, wherein said cost functions are in terms of critical area contributions, and wherein said critical area contributions comprise a measure of electrical fault characteristics of said spacing between said edges in said integrated circuit design;

d) optimizing said positions and lengths of said edges in said integrated circuit design to reduce crit-ical area contribution cost in a first direction across said integrated circuit design to produce a revised integrated circuit design; and

e) repeating steps b-d with said revised integrated circuit design in a second direction.

[c13] 13. The method in claim 15, wherein said process of as-sociating said cost functions comprises mapping points in said spacing between said edges in said integrated

circuit design up to when the size of defects located at said points triggers an electrical fault between said edges in said integrated circuit design, wherein said mapping forms Voronoi cells.

[c14] 14. The method in claim 16, wherein said process of associating said cost functions further comprises using a normal vector representing said Voronoi cells defined in terms of said variables.

[c15] 15. The method in claim 15, wherein said process of associating said cost functions further comprises identifying Voronoi bisectors where Voronoi cells meet.

[c16] 16. The method in claim 18, wherein said Voronoi bisectors are defined by vertices at the ends of said Voronoi bisectors; and wherein said vertices are defined in terms of said variables.

[c17] 17. The method in claim 19, wherein said cost function calculates critical area contributions of said Voronoi bisectors as said variables change as the layout of said integrated circuit design changes.

[c18] 18. A service for calculating critical area in an integrated circuit design, said service comprising:

inputting an integrated circuit design;

associating variables with the positions of edges in

said integrated circuit design; and

associating cost functions of said variables with spacing between said edges in said integrated circuit design;

wherein said cost functions are in terms of critical area contributions, and

wherein said critical area contributions comprise a measure of electrical fault characteristics of said spacing between said edges in said integrated circuit design.

[c19] 19. The service in claim 22, wherein said process of associating said cost functions comprises mapping points in said spacing between said edges in said integrated circuit design up to when the size of defects located at said points triggers an electrical fault between said edges in said integrated circuit design, wherein said mapping forms Voronoi cells.

[c20] 20. The service in claim 23, wherein said process of associating said cost functions further comprises using a normal vector representing said Voronoi cells defined in terms of said variables.

[c21] 21. The service in claim 22, wherein said process of associating said cost functions further comprises identifying Voronoi bisectors where Voronoi cells meet.

[c22] 22. The service in claim 25, wherein said Voronoi bisectors are defined by vertices at the ends of said Voronoi bisectors; and wherein said vertices are defined in terms of said variables.

[c23] 23. The service in claim 26, wherein said cost function calculates critical area contributions of said Voronoi bisectors as said variables change as the layout of said integrated circuit design changes.

[c24] 24. A program storage device readable by computer, tangibly embodied a program of instructions executable by said computer for performing a method of calculating critical area in an integrated circuit design, said method comprising:

inputting an integrated circuit design;

associating variables with the positions of edges in said integrated circuit design; and

associating cost functions of said variables with spacing between said edges in said integrated circuit design;

wherein said cost functions are in terms of critical area contributions; and

wherein said critical area contributions comprise a measure of electrical fault characteristics of said spacing between said edges in said integrated circuit

design.

[c25] 25. The program storage device in claim 29, wherein said process of associating said cost functions comprises mapping points in said spacing between said edges in said integrated circuit design up to when the size of defects located at said points triggers an electrical fault between said edges in said integrated circuit design, wherein said mapping forms Voronoi cells.

[c26] 26. The program storage device in claim 30, wherein said process of associating said cost functions further comprises using a normal vector representing said Voronoi cells defined in terms of said variables.

[c27] 27. The program storage device in claim 29, wherein said process of associating said cost functions further comprises identifying Voronoi bisectors where Voronoi cells meet.

[c28] 28. The program storage device in claim 32, wherein said Voronoi bisectors are defined by vertices at the ends of said Voronoi bisectors; and wherein said vertices are defined in terms of said variables.

[c29] 29. The program storage device in claim 33, wherein said cost function calculates critical area contributions of said Voronoi bisectors as said variables change as the

layout of said integrated circuit design changes.

[c30] 30.A system for calculating critical area in an integrated circuit design, said system comprising:

means for inputting an integrated circuit design;

means for associating variables with the positions of edges in said integrated circuit design; and

means for associating cost functions of said variables with spacing between said edges in said integrated circuit design;

wherein said cost functions are in terms of critical area contributions, and

wherein said critical area contributions comprise a measure of electrical fault characteristics of said spacing between said edges in said integrated circuit design.

[c31] 31. A method of optimizing critical area in an integrated circuit design, said method comprising:

inputting an initial integrated circuit design;

associating variables with the positions of edges in said integrated circuit design;

associating cost functions of said variables with spacing between said edges in said integrated circuit design; and

optimizing said positions and length of said edges in said integrated circuit design to reduce critical area

contribution cost in a first direction across said integrated circuit design to produce a revised integrated circuit design.

[c32] 32. The method in claim 37, wherein said process of associating said cost functions comprises mapping points in said spacing between said edges in said integrated circuit design up to when the size of defects located at said points triggers an electrical fault between said edges in said integrated circuit design, wherein said mapping forms Voronoi cells.

[c33] 33. The method in claim 38, wherein said process of associating said cost functions further comprises using a normal vector representing said Voronoi cells defined in terms of said variables.

[c34] 34. The method in claim 37, wherein said process of associating said cost functions further comprises identifying Voronoi bisectors where Voronoi cells meet.

[c35] 35. The method in claim 40, wherein said Voronoi bisectors are defined by vertices at the ends of said Voronoi bisectors; and wherein said vertices are defined in terms of said variables.

[c36] 36. The method in claim 41, wherein said cost function calculates critical area contributions of said Voronoi bi-

sectors as said variables change as the layout of said integrated circuit design changes.